FIG. 1A

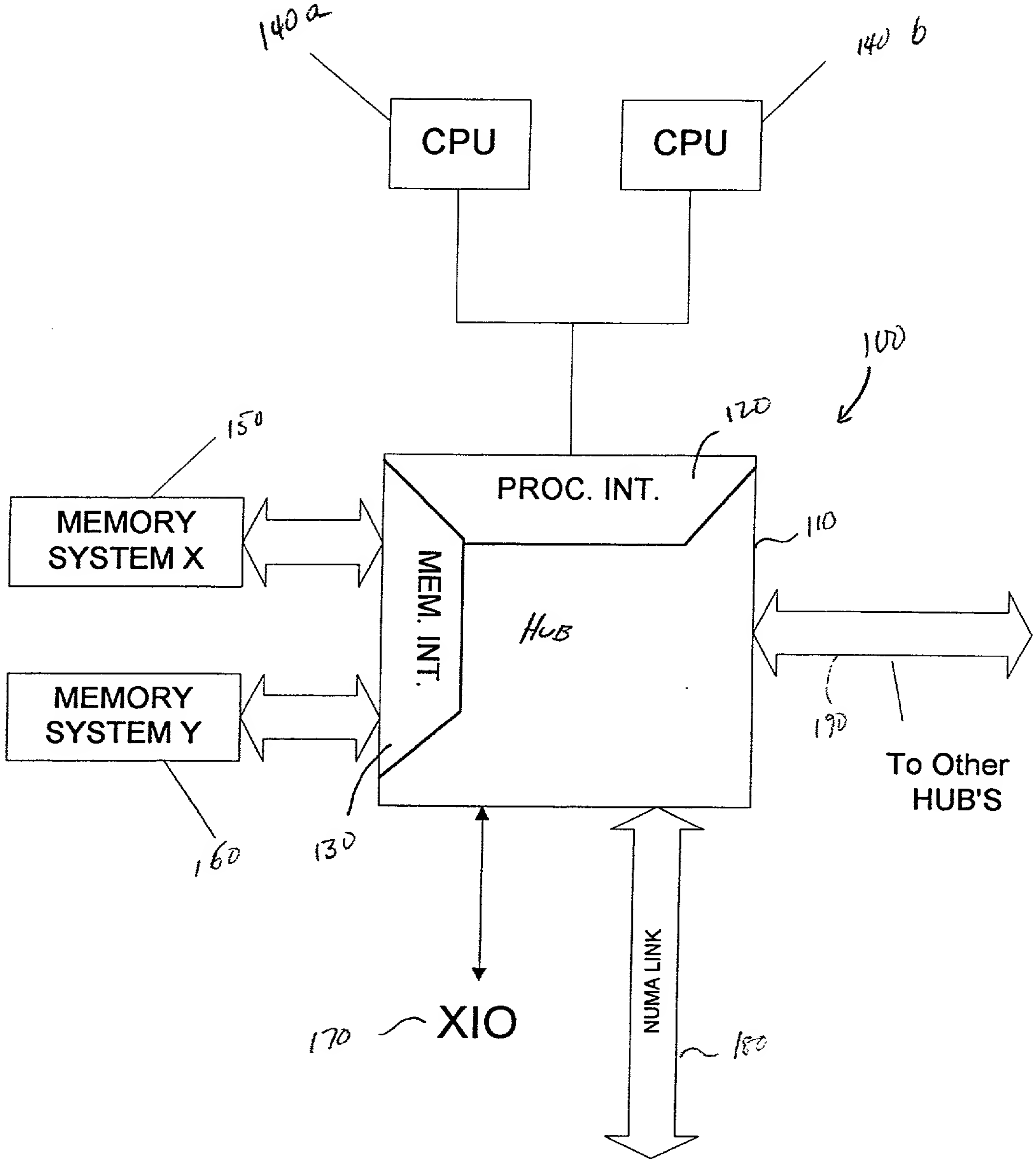
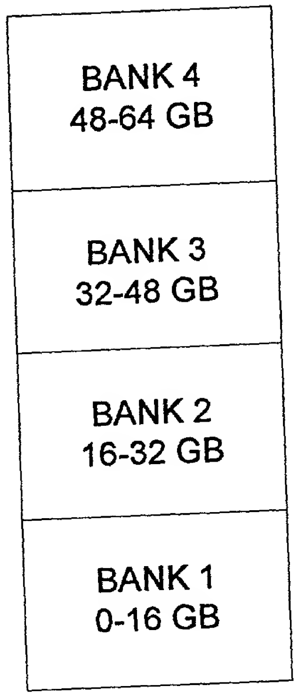

140a
140b
CPU
CPU
100
120
150
PROC. INT.
110
MEMORY SYSTEM X
MEM. INT.
HUB
MEMORY SYSTEM Y
190
To Other HUB'S
160
130
NUMA LINK
170
XIO
180

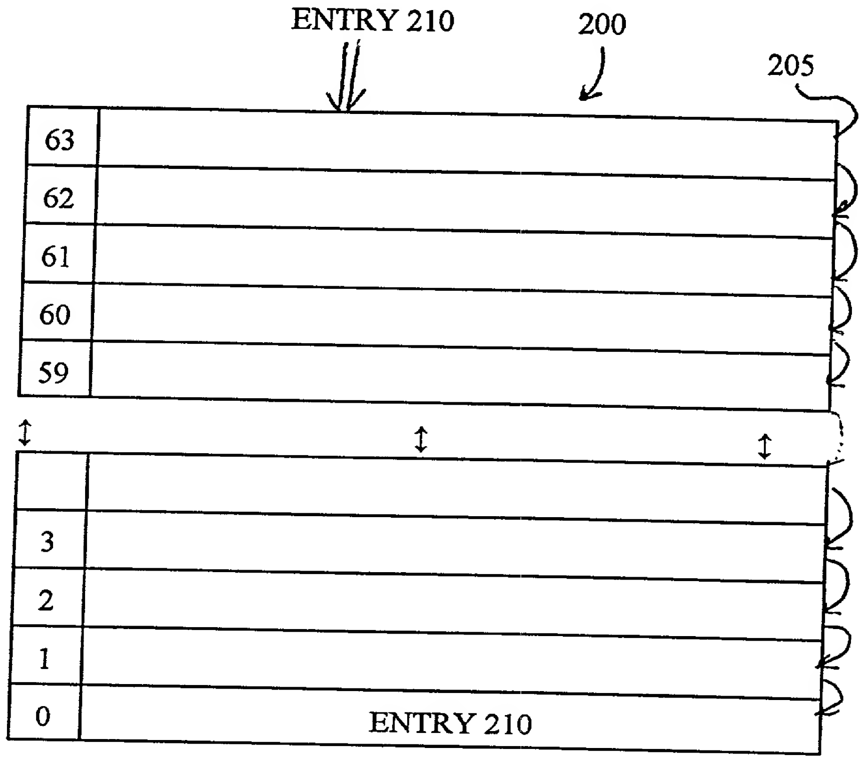
FIG. 1B



36 BIT MEMORY ADDRESS

BITS 35:34 - BANK SELECT
BITS 33:0 - ADDRESS WITHIN BANK

FIG 2A


ENTRY 210
200
205
63
62
61
60
59
3
2
1
0
ENTRY 210

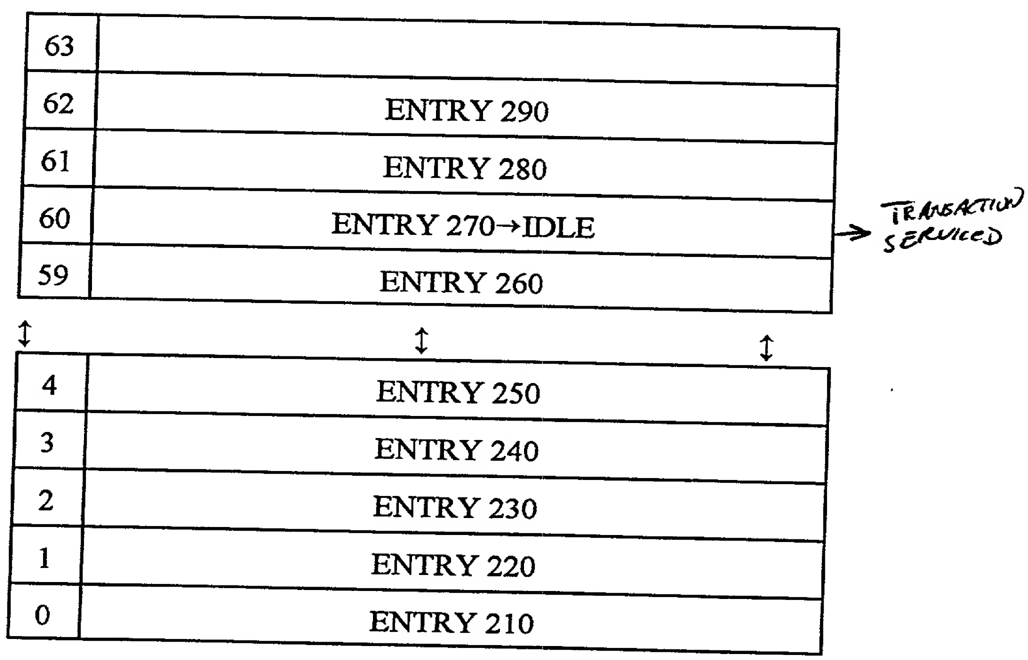

63
62
ENTRY 290
61
ENTRY 280
60
ENTRY 270→IDLE
59
ENTRY 260
TRANSACTION SERVICED
4
ENTRY 250
3
ENTRY 240
2
ENTRY 230
1
ENTRY 220
0
ENTRY 210

FIG. 2B

Fig 2C

63	
62	
61	ENTRY 290
60	ENTRY 280
59	ENTRY 260
↕	↕
4	ENTRY 250
3	ENTRY 240
2	ENTRY 230
1	ENTRY 220
0	ENTRY 210

Fig 4.

STATE	R/W	CHAIN OK	BANK FREE	OP READY	TRANSACTION
460	450	440	430	420	410

FIG. 3

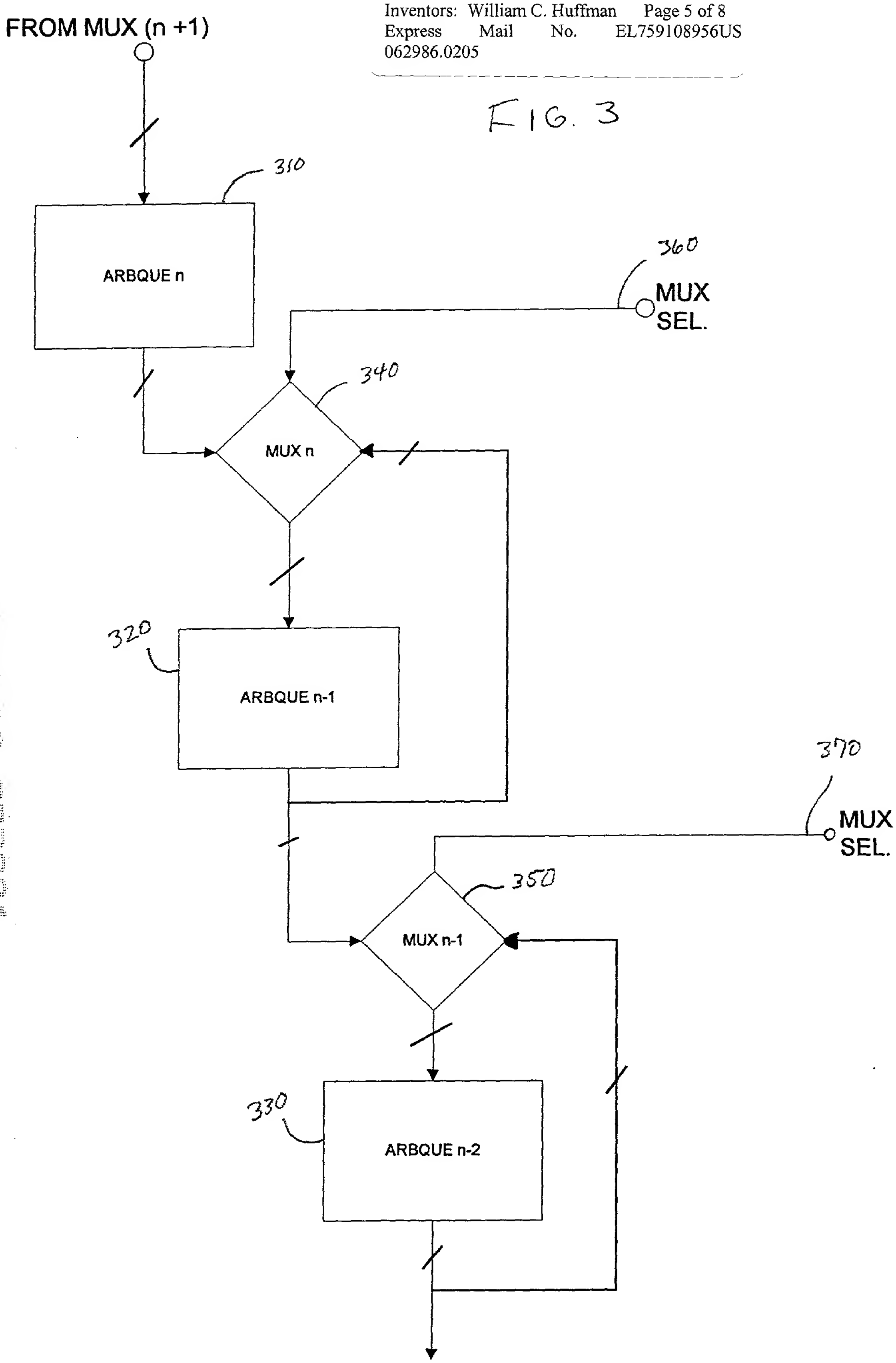

FROM MUX (n +1)
310
ARBQUE n
360
MUX SEL.
340
MUX n
320
ARBQUE n-1
370
MUX SEL.
350
MUX n-1
330
ARBQUE n-2

FIG 5

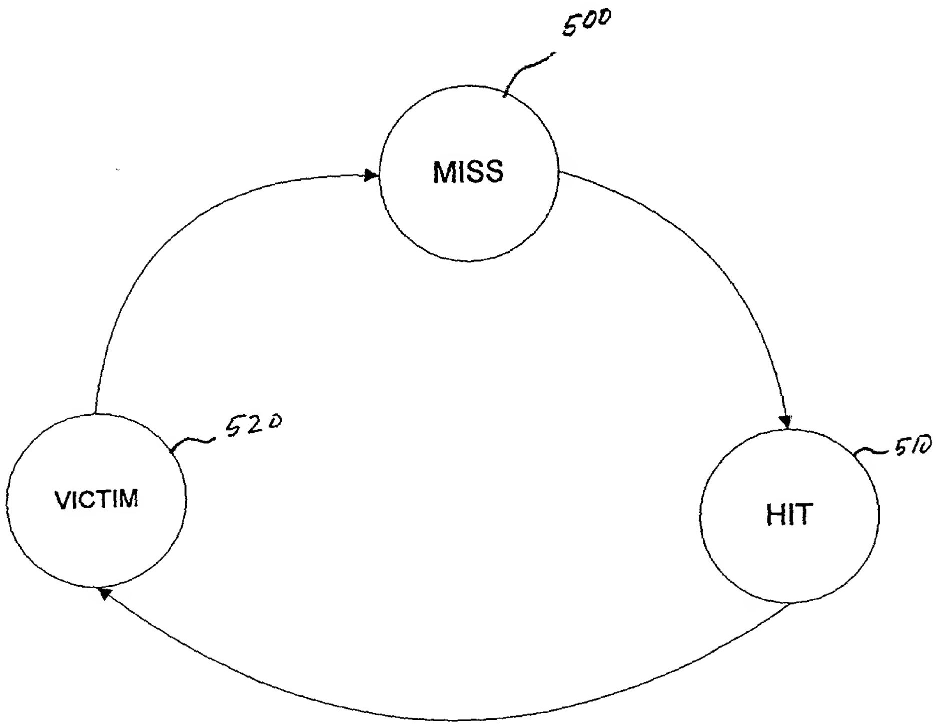


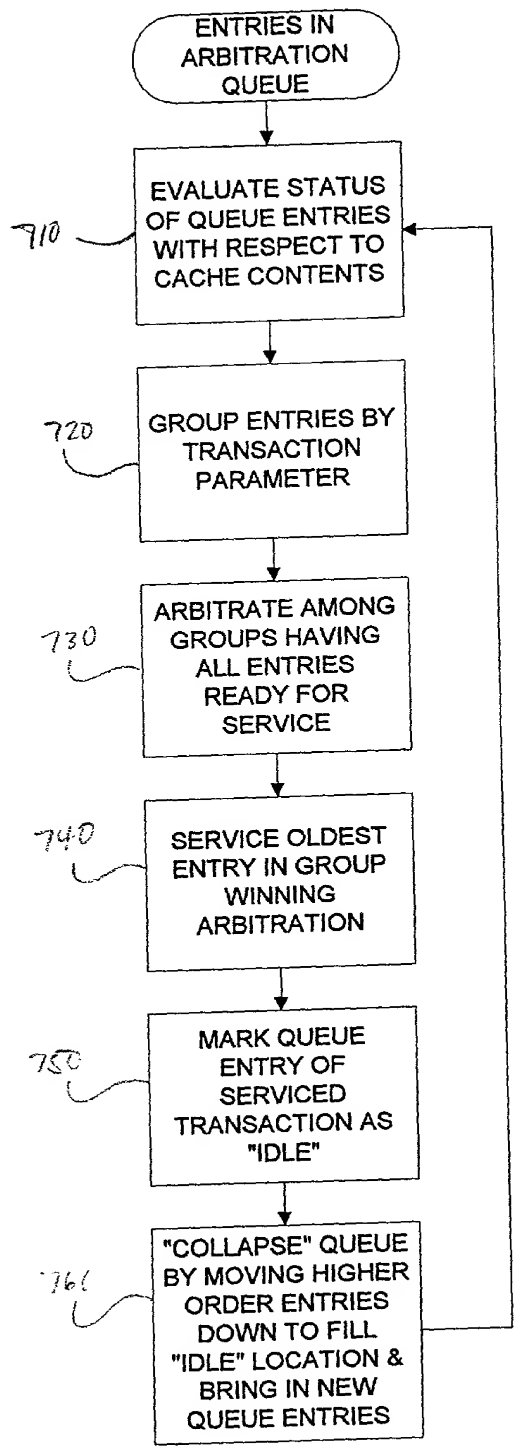
Fig. 6

600 610 620 630 640 650 660

DRAM Direction Arbitration Policy Table

Read	Write	Urgent Write	Follows Read	Follows Write	Direction Threshold	Arbitrate For
x	0	0	x	x	x	Read
0	x	1	x	x	x	Write
0	1	0	1	0	x	Read
0	1	0	0	x	x	Write
1	1	0	x	0	x	Read
1	1	0	0	1	0	Write
1	1	0	0	1	1	Read
1	x	1	0	x	x	Write
1	x	1	1	0	0	Read
1	x	1	1	0	1	Write

FIG 7


ENTRIES IN ARBITRATION QUEUE
710
EVALUATE STATUS OF QUEUE ENTRIES WITH RESPECT TO CACHE CONTENTS
720
GROUP ENTRIES BY TRANSACTION PARAMETER
730
ARBITRATE AMONG GROUPS HAVING ALL ENTRIES READY FOR SERVICE
740
SERVICE OLDEST ENTRY IN GROUP WINNING ARBITRATION
750
MARK QUEUE ENTRY OF SERVICED TRANSACTION AS "IDLE"
760
"COLLAPSE" QUEUE BY MOVING HIGHER ORDER ENTRIES DOWN TO FILL "IDLE" LOCATION & BRING IN NEW QUEUE ENTRIES